PCI30FG Series

PCI PnP Analog Input Board User's Manual

PCI30G, PCI30GA, PCI30G32, PCI30GA32
PCI30F, PCI30FA, PCI30F32, PCI30FA32

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Analog Input Boards

Data Acquisition and Process Control

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1 Introduction

The PCI30FG series are 32-bit bit PCI bus architecture data acquisition boards. They are available in two basic models, the G and F series. They can samples at 100kHz or 330kHz respectively. Addition to analog input, they also have analog output, digital input/output and counter-timer capabilities. For this reason the PCI30FG is an excellent all purpose data acquisition device with extensive analog input capabilities.

Features

The PCI30FG does have some very unique features and are short listed below:

- 32-bit PCI bus Revision 2.1 compliant
- 8/16 differential or 16/32 single-ended A/D inputs
- 2K word A/D FIFO
- Auto channel scanning
- Software controlled input ranges and gains
- 3 x 8-bit I/O ports
- 4 x 16-bit user counter-timers

Applications

The PCI30FG can be used in the following applications:

- Voltage monitoring
- Voltage control
- FFT signal calculation
- General process control
- Frequency measurement
- Pulse counting

Key Specifications

- A/D resolution: 12-bits
- D/A resolution: 12-bits
- DIO width: 8-bits
- CT width: 16-bits
- A/D non-linearity: less than ±0.75LSB
- A/D ranges: ±5V, ±10V, 0-10V
- A/D scan rate: 100kHz or 330kHz
- A/D, D/A interfaces via a 50 way SCSI right angle female centronics connector
- Digital I/O, Counter-timer via IDC40 Header

Software Support

The PCI30FG is supported by EDR Enhanced and comes with an extensive range of examples. The software will help you to get your hardware going very quickly. It also makes it easy to develop complicated control applications quickly. All operating system drivers, utility and test software are supplied on a CD-Rom.

2

2 Installation

This chapter describes how to install and configure the PCI30FG for the first time. Minimal configuration is necessary; almost all settings are done through software. The PCI BIOS will assign an I/O base address and interrupt level.

Package

PCI30FG package will contain the following:

- PCI30FG PCI board
- EDR Enhanced Software Development Kit CD-Rom

Hardware Installation

This section will describe how to install your PCI30FG into your computer.

- Switch off the computer and disconnect from power socket.

Failure to disconnect all power cables can result in hazardous conditions, as there may be dangerous voltage levels present in externally connected cables.

- Remove the cover of the PC.
- Choose any open PCI slot and insert PCI30FG.
- Insert bracket screw and ensure that the board sits firmly in the PCI socket.
- Install digital I/O connector cable.
- Replace the cover of the PC.
- Reconnect all power cables and switch the power on.
- The hardware installation is now completed.

Software Installation

Windows 98

Installing the Windows 98 device driver is a very straightforward task. Because it is plug and play Windows will detect the PCI30FG as soon as it is installed. No setup is necessary. You simply only have to supply Windows with a device driver.

Wait until Windows detects the new hardware

Add New Hardware Wizard
This wizard searches for new drivers for:
PCI System Peripheral
A device driver is a software program that makes a hardware device work.
< Back
Next >
Cancel

Figure 2-1 Add New Hardware Wizard Step1

Select Next

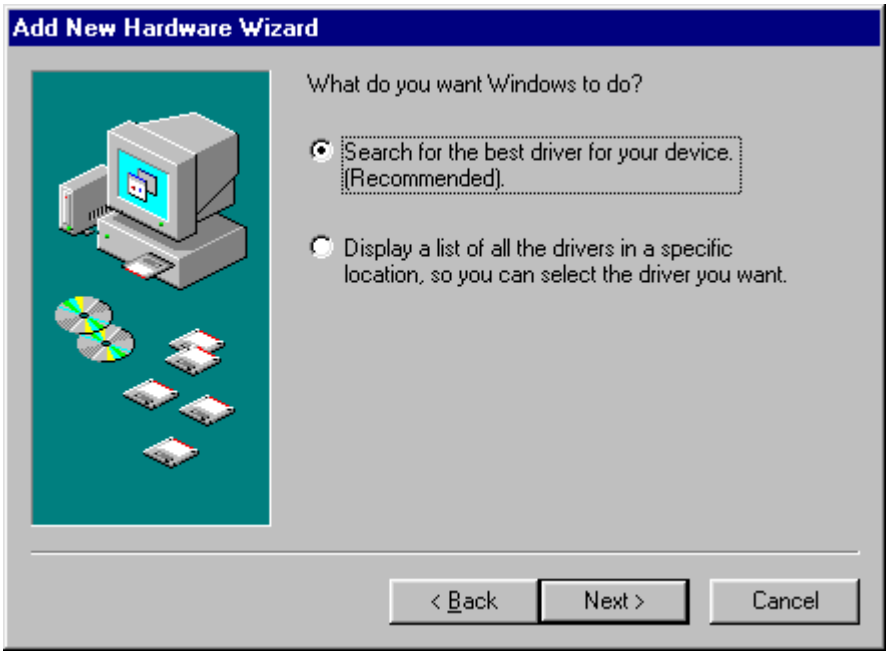

Add New Hardware Wizard
What do you want Windows to do?
Search for the best driver for your device. (Recommended).
Display a list of all the drivers in a specific location, so you can select the driver you want.
< Back
Next >
Cancel

Figure 2-2 Add New Hardware Wizard Step2

Select default option, search for best driver and select next

Add New Hardware Wizard
Windows will search for new drivers in its driver database on your hard drive, and in any of the following selected locations. Click Next to start the search.
Floppy disk drives
CD-ROM drive
Microsoft Windows Update
Specify a location:
E:\DRIVERS\WIN9X\PCI36C
Browse...
< Back
Next >
Cancel

Figure 2-3 Add New Hardware Wizard Step3

Select specify a location and enter the directory location of the driver on your EDR Enhanced SDK CD Rom
<CDROM>\EDRE\DRIVERS\WDM\PCI30FG
Select Next to proceed

Add New Hardware Wizard
Windows driver file search for the device:
PCI36C Digital I/O Board
Windows is now ready to install the best driver for this device. Click Back to select a different driver, or click Next to continue.
Location of driver:
A:\PCI36C.INF
< Back
Next >
Cancel

Figure 2-4 Add New Hardware Wizard Step4

Windows should have detected the proper driver and ready to install it. Select Next to proceed.

Add New Hardware Wizard
PCI36C Digital I/O Board
Windows has finished installing the software that your new hardware device requires.
< Back
Finish
Cancel

Figure 2-5 Add New Hardware Wizard Step5

Click on the finish button to complete the installation.
Click Yes to restart your computer.

System Settings Change
To finish setting up your new hardware, you must restart your computer.
Do you want to restart your computer now?
Yes
No

Figure 2-6 Restart Your Computer

Post installation

After your installation was complete there is a few steps that can be followed to check that your installation was successful.

- First make sure that the driver is working properly by opening the *system folder* in the control panel.
- Check under the system device list if your board is listed and working properly. See picture below.

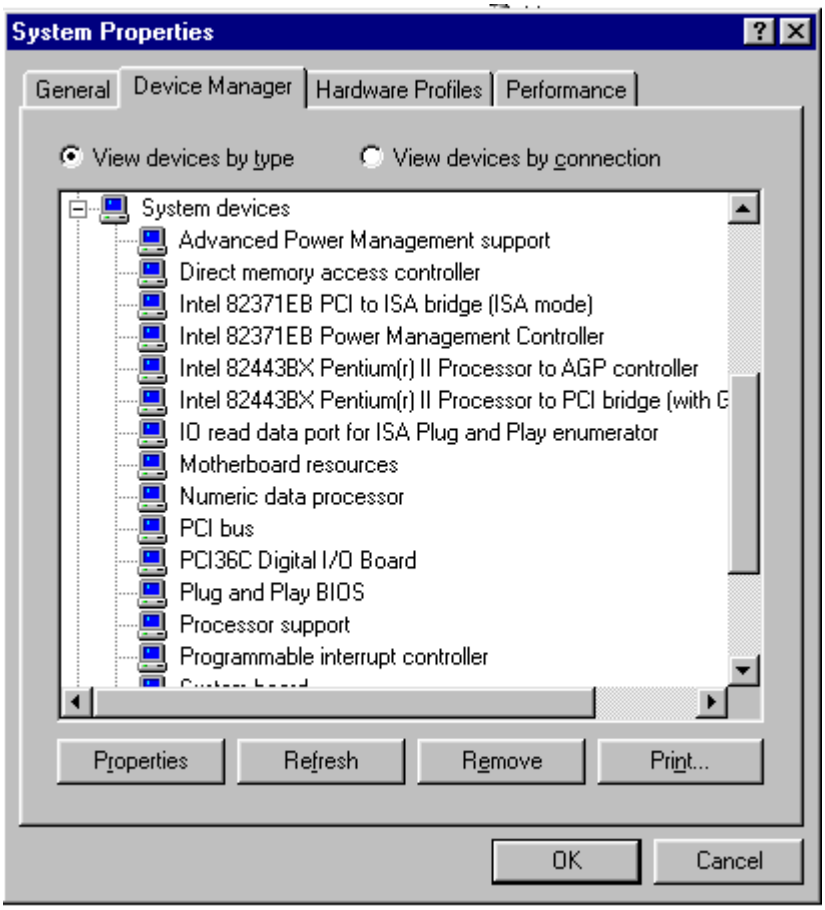


Figure 2-7 System Properties

- Clearly you can see that the PCI36C is listed and working properly.

- Further open the control panel and then the *EagleDAQ* folder. This dialog should list all installed hardware. Verify your board's properties on this dialog. See picture below

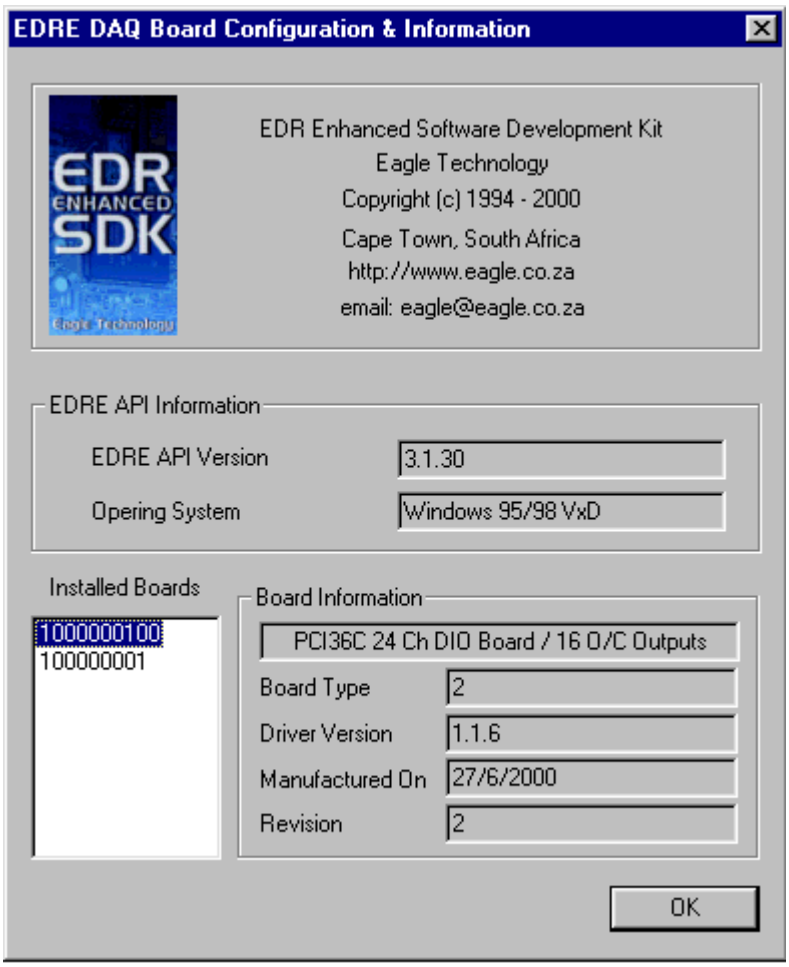


Figure 2-8 EagleDAQ

Now the first part of your installation has been completed and ready to install the EDR Enhanced Software Development Kit.

- Run ***setup.exe*** found on the EDR Enhanced SDK CD-Rom and follow the on screen instructions

Windows NT/2000

Windows NT/2000 does not require any special setup procedure. The Windows NT driver does not support plug and play. If Windows 2000 detects a new device simply install a default driver, or so called placeholder.

To install the Windows NT/2000 drivers simply run ***setup.exe*** on the EDR Enhanced CD-Rom. This will automatically install the device drivers. Restart your computer when done. Open the *EagleDAQ* folder in the control panel to check if your installation was successful. Figure 2-8 shows a successful installation.

Configuration

Only the PCI30Gx series allows one manual setting. The PCI30Gx series has one jumper, LK1, to change the voltage span. The figure below shows the two different jumper settings.

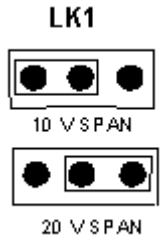


Figure 2-9 A/D Span Jumper

Accessories

The PCI30FG does have a wide variety of accessories that it can be connected too. See chapter on accessories.

3

3 Interconnections

The PCI30FG is designed so that there is a connector for analog signals and digital signals. The analog connector is on the bracket attached to the board and the other a connector on the PCB internal to the PC.

External Connectors

The PCI30FG does have two connectors, a SCSI-II-50 female centronics and an IDC40 male. The ICD40M can also be extended to the computer casing by making use of an extender cable and bracket that is supplied with the PCI30FG package. The extender cable will make the digital I/O and counter-timer signals available outside the computer casing. The connector is a DB37 male.

Pin Assignments

The table below shows the pin assignments for the PCI30FG.

Pin	Name	Pin	Name
1	+5V	26	+12V
2	EXT TRIG	27	-12V
3	DGND	28	EXT CLK
4	DAC3	29	SENSE3
5	DAC2	30	SENSE2
6	DAC1	31	SENSE1
7	DAC0	32	SENSE0
8	AGND	33	AGND
9	AGND	34	AGND
10	CHAN0	35	CHAN1
11	CHAN2	36	CHAN3
12	CHAN4	37	CHAN5
13	CHAN6	38	CHAN7
14	CHAN8	39	CHAN9
15	CHAN10	40	CHAN11
16	CHAN12	41	CHAN13

17	CHAN14	42	CHAN15
18	CHAN16	43	CHAN17
19	CHAN18	44	CHAN19
20	CHAN20	45	CHAN21
21	CHAN22	46	CHAN23
22	CHAN24	47	CHAN25
23	CHAN26	48	CHAN27
24	CHAN28	49	CHAN29
25	CHAN30	50	CHAN31

Table 3-1 External Analog Connector - SCSI-II-50F CENT

Pin	Name	Pin	Name
1	PA0	2	PA1
3	PA2	4	PA3
5	PA4	6	PA5
7	PA6	8	PA7
9	PB0	10	PB1
11	PB2	12	PB3
13	PB4	14	PB5
15	PB6	16	PB7
17	PC0	18	PC1
19	PC2	20	PC3
21	PC4	22	PC5
23	PC6	24	PC7
25	DGND	26	CLK2
27	CNT0	28	OUT2
29	COUT0	30	CGTE0
31	CGTE1	32	CNT1
33	CNT2	34	COUT1
35	COUT2	36	CGTE2
37	+5V	38	DGND
39	DGND	40	DGND

Table 3-2 Internal DIO/CT Connector – IDC-40M

Pin	Name	Pin	Name
1	PA0	20	PA1
2	PA2	21	PA3
3	PA4	22	PA5
4	PA6	23	PA7
5	PB0	24	PB1
6	PB2	25	PB3
7	PB4	26	PB5
8	PB6	27	PB7
9	PC0	28	PC1
10	PC2	29	PC3
11	PC4	30	PC5
12	PC6	31	PC7
13	DGND	32	CLK2
14	CNT0	33	OUT2
15	COUT0	34	CGTE0
16	CGTE1	35	CNT1
17	CNT2	36	COUT1
18	COUT2	37	CGTE2
19	+5V		

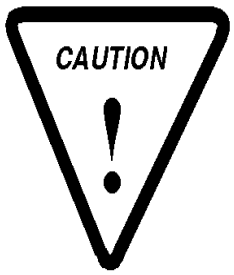
Table 3-3 External DIO/CT Connector - DB-37M

Signal Definitions

This sections deal with all the signals abbreviations.

Signal	Description
CHAN0-31	Analog input channel
DAC0-3	Analog output channel
SENSE0-3	Sensing line for analog output channel
PA0-7	Port A on PPI
PB0-7	Port B on PPI
PC0-7	Port C on PPI
CNT0-2	User counter clock input
COUT0-2	User counter clock output
CGTE0-2	User counter gate
CLK2	Internal counter input
OUT2	Internal counter output

Table 3-4 Signal definitions



OVERLOADING ANY ANALOGUE INPUT BY MORE THAN 10% MAY CAUSE OTHER INPUT CHANNELS TO BECOME INACCURATE OR NOISY. FOR PCI30FG INPUTS OPERATING AT MAXIMUM GAIN, THIS CORRESPONDS TO AN INPUT VOLTAGE OF 5.5 mV.

Analog Input

Analog signals are connected either as single ended or differential inputs.

Single Ended Inputs

With single ended inputs, connections share a common low reference that is connected to analog ground. See figure below.

The advantage of such a connection is that you have a maximum number of inputs. Its major disadvantage is the loss of common mode rejection obtainable from differential mode. Single ended inputs are very sensitive to noise lead lengths should be kept as short as possible.

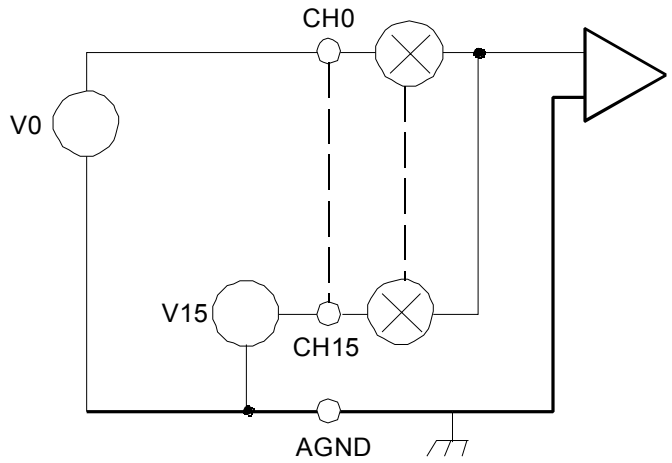


Figure 3-1 Single ended analog input

Differential Inputs

In differential input mode two multiplexer switches per channel are used. The A/D converter measures the difference in potential between the two channels.

Channels are paired to form a single differential input. Channel 0 and channel 8 is used as channel 0, channels 1 and 9 etc. To connect see diagram below. It is also very important to know that each return connection must be referenced to analog ground.

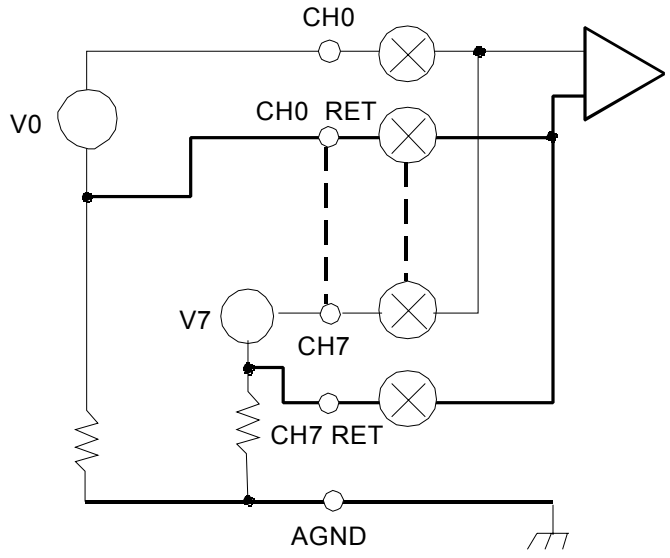


Figure 3-2 Differential Analog Inputs

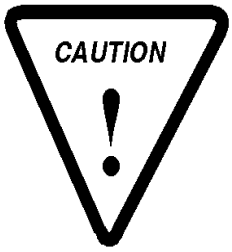
In differential mode, all signal inputs to the PCI30FG must be referred to ground. This can be done by connecting a 1 to 10 kΣ resistor from the low end of each input to ground.

Analog Output

The analog outputs come with sense lines and it is important to make sure that they are connected to the correct channel. If left unconnected the output will simple float at +10V or –10V. The analog output range is ±10V and is fully software configurable. The EDR Enhanced driver support auto ranging and will always select the range with the best possible resolution. For normal operation simply connect SENSE0 to DAC0.

Digital Input/Output

The PCI30FG has got 3x8-bit digital I/O ports that are fully configurable as inputs or outputs. The digital I/O uses a chip that is fully compatible with the Intel 8255 programmable peripheral interface. Make sure not to overload the PPI because it will cause serious damage and will need to be repaired.



OVERLOADING ANY DIGITAL I/O LINE WILL CAUSE SERIOUS DAMAGE TO THE DIGITAL I/O CHIP. OPERATING OUTSIDE THE TTL VOLTAGE RANGE WILL CAUSE PERMANENT DAMAGE TO THE DIGITAL I/O CONTROL CIRCUIT.

Counter-Timer

There are six counter-timers on the PCI30FG of which four are available for the user. Two are used for A/D timing. The timers are compatible with the Intel 8254 counter-timer device. The 8254 counter-timer datasheets can be used as reference for configuring the counter-timer sub-system.

There is no onboard clock for the user counter-timers and an external clock is required.

4 Programming Guide

The PCI30FG is supplied with a complete software development kit. EDR Enhanced (EDRE SDK) comes with drivers for many operating systems and a common application program interface (API). The API also serves as a hardware abstraction layer (HAL) between the control application and the hardware. The EDRE API make it possible to write one application that can be used on all hardware with common sub-systems.

The PCI30FG can also be programmed at register level, but it is not recommended. A detailed knowledge of the PCI30FG is needed and some knowledge about programming Plug and Play PCI devices. We recommend that you only make use of the software provided by Eagle Technology.

EDR Enhanced API

The EDR Enhanced SDK comes with both ActiveX controls and a Windows DLL API. Examples are provided in many different languages and serve as tutorials. EDRE is also supplied with a software manual and user's guide.

The EDRE API hides the complexity of the hardware and makes it really easy to program the PCI30FG. It has got functions for each basic sub-system and is real easy to learn.

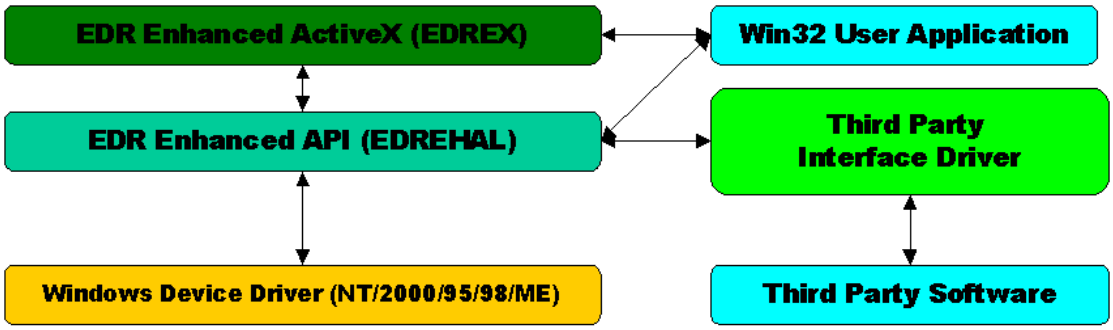


Figure 4-A EDR Enhanced Design

Digital Inputs/Outputs

The PCI30FG has 24 digital I/O lines, configured as 3 x 8-bit ports. The EDRE API supports auto direction configuration. By writing to or reading from a port, it is automatically configured as an output or input. A port is defined as a collection of simultaneous configurable entities. Thus in the case of the PCI30FG each port is only 8-bits wide.

Reading the Digital Inputs

A single call is necessary to read a digital I/O port.

API-CALL

Long EDRE_DioRead(ulng Sn, ulng Port, ulng *Value)

The serial number, port, and a pointer to variable to hold the result must be passed by the calling function. A return code will indicate if any errors occurred.

ACTIVEX CALL

Long EDREDioX.Read(long Port)

Only the port-number needs to be passed and the returned value will either hold an error or the value read. If the value is negative an error did occur.

Writing to the Digital Outputs

A single call is necessary to write to a digital I/O port.

API-CALL

Long EDRE_DioWrite(ulng Sn, ulng Port, ulng Value)

The serial number, port, and a value must be passed by the calling function. A return code will indicate if any errors occurred.

ACTIVEX CALL

Long EDREDioX.Write(long Por, ulng Value)

The port number and value to be written needs to be passed and the returned value holds an error or the value read. If the value is negative an error did occur.

Counters

The counter sub-system is supported by functions to Write, Read and Configure. There are 4 counters that are available to the user and are compatible with the industry standard 8254 counter-timer. The table below shows all counters and their assigned function on the board. Please note that only some are available for the user. The 8254 datasheet has more information on the counter-timer modes.

Counter	Software Assigned Number	Description
0	N/A	ADC clock
1	N/A	ADC prescaler
2	3	User Counter 3
3	0	User Counter 0
4	1	User Counter 1
5	2	User Counter 2

Table 4-1 Counter Assignment

Writing the initial counter value

A single call is necessary to write a counter's initial load value.

API-CALL

Long EDRE_CTWrite(ulng Sn, ulng Ct, ulng Value)

The serial number, counter-number, and a value must be passed by the calling function. A return code will indicate if any errors occurred.

ACTIVEX CALL

Long EDRECTX.Write(long Port, ulng Value)

The port number and value to be written needs to be passed and the returned value holds an error or the value read. If the value is negative an error did occur.

Reading a counter

A single call is necessary to read a counter's current value.

API-CALL

Long EDRE_CTRead(ulng Sn, ulng Ct, pulng Value)

The serial number, counter-number, and a pointer must be passed by the calling function. A return code will indicate if any errors occurred. The value buffer will hold the value read from the counter.

ACTIVEX CALL

Long EDRECTX.Read(long Port)

The port number needs to be passed. The returned value will either hold the error code or the value read from the counter. If negative it means an error occurred, otherwise it is the value read from the counter.

Configuring a counter

A single call is necessary to configure a counter. An external clock must clock the first three counters, but the internal 8MHz clock clocks the fourth counter.

API-CALL

Long EDRE_CTConfig(ulng Sn, ulng Ct, ulng Mode, ulng Type, ulng ClkSrc, ulng GateSrc)

The serial number, counter-number, mode, type, clock source and gate source is needed to specify a counter's configuration. A return code will indicate if any errors occurred.

ACTIVEX CALL

Long EDRECTX.Configure(long ct, long mode, long type, ulng source, ulng gate)

The counter-number, mode, type, clock source and gate source is needed to specify a counter's configuration. A return code will indicate if any errors occurred.

Only the counter mode parameter is used by the PCI30FG. The table below shows the options for each parameter.

Parameter	Description
Sn	Serial Number
Ct	Counter Number: 0 : User Counter 0 1 : User Counter 1 2 : User Counter 2 3 : User Counter 3
Mode	8254 Counter Mode. See 8254 datasheet for details
Type	Not Used
Source	Not Used
Gate	Not Used

Table 4-2 Counter Configuration

How to latch all counters

The 8254 counters support a function where all counters can be latched at the same time. The PCI30FG driver supports this function through a query call to the driver. This will only work on the first 3 user counters.

Example:
Unsigned long sn=1000000001
EDRE_Query(sn,CTLATCALL=302,0)

Analog Output

The PCI30FG-A version has 4 x 12-bit DAC channels that support single write.

Writing to a DAC channel

A single call is necessary to set a voltage on a DAC channel.

API-CALL

Long EDRE_DAWrite (ulng Sn, ulng Channel, long uVoltage)

The serial number, DAC channel and micro-voltage is needed to set a DAC channel's voltage. A return code will indicate if any errors occurred.

ACTIVEX CALL

Long EDREDAX.Write (long Channel, long uVoltage)

The DAC channel and micro-voltage is needed to set a DAC channel's voltage. A return code will indicate if any errors occurred.

Analog Input

The PCI30FG's ADC subsystem is fully configurable and supports single channel reading and out scanning. While scanning a channel list and gain list can be provided. Channels are scanned in the same sequence provided in the channel list.

Reading a single voltage from a channel

To read a single ADC channel you need to know the voltage range and gain.

API-CALL

Long EDRE_ADSingle (ulng Sn, ulng Channel, ulng Gain, ulng Range, plong uVoltage)

Parameter	Type	Description
Sn	Unsigned long	Board's serial number
Channel	Unsigned long	ADC Channel
Gain	Unsigned long	0: Gain x 1 1: Gain x 10 2: Gain x 100 3: Gain x 1000
Range	Unsigned long	0: -5V to +5V, Single Ended 1: 0 to +10V, Single Ended 2: -10V to +10V, Single Ended 3: -5V to +5V, Differential 4: 0 to +10V, Differential 5: -10V to +10V, Differential
uVoltage	Pointer to a long	Voltage read from channel
Return	Long	Error Code

ACTIVEX CALL

Long EDREADX.SingleRead (long Channel)

Parameter	Type	Description
Channel	Long	ADC Channel
Return	Long	Voltage returned from channel.

Make sure to set the *Gain* and *Range* properties of the ADC ActiveX control. This will in turn set the range and gain when reading the ADC channel.

Configuring the ADC subsystem for scanning

This is the most complicated part of configuring the PCI703 for auto scanning. Make sure that you use the correct format when applying the channel list configuration. There are many loopholes and care should be taken when implementing code to configure the PCI703.

API-CALL

Long EDRE_ADConfig (ulng Sn, pulng Freq, ulng ClkSrc, ulng Burst, ulng Range, pulng ChanList, pulng GainList, ulng ListSize)

The following parameters must be specified when configuring the ADC sub-system.

Parameter	Type	Description
Sn	Unsigned long	Board's serial number.
Freq	Pointer to an unsigned long	Sampling frequency. The actual sampling frequency will be returned with this parameter.
ClkSrc	Unsigned long	0: Internal and to External Gate 1: Internal 2: External Clock 3: External Clock and Gate
Burst	Unsigned long	0: Normal Mode 1: Burst Mode
Range	Unsigned long	0: -5V to +5V, Single Ended 1: 0 to +10V, Single Ended 2: -10V to +10V, Single Ended 3: -5V to +5V, Differential 4: 0 to +10V, Differential 5: -10V to +10V, Differential
ChanList	Pointer to an unsigned long	This is an array of unsigned longs that contains the gains of channels to be sampled when scanning the ADC sub-system. The max size of the channel list is 64.
GainList	Pointer to an unsigned long	This is an array of unsigned longs that contains the channels to be sampled when scanning the ADC sub-system. The max size of the channel list is half the FIFO depth.
ListSize	Unsigned long	This parameter determines the length the two previous arrays. This is also the depth of the channel list that is programmed to the board.

ACTIVEX CALL

Long EDREADX.Configure (plong Channels, plong Gains, long ListSize)

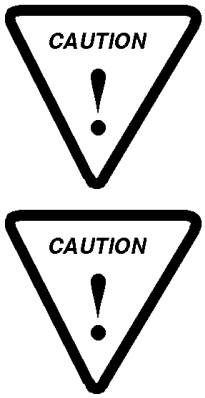
Parameter	Type	Description
Channels	Pointer to an unsigned long	This is an array of unsigned longs that contains the gains of channels to be sampled when scanning the ADC sub-system. The max size of the channel list is half the FIFO depth.
Gains	Pointer to an unsigned long	This is an array of unsigned longs that contains the channels to be sampled when scanning the ADC sub-system. The max size of the channel list is half the FIFO depth.
ListSize	Unsigned long	This parameter determines the length the two previous arrays. This is also the depth of the channel list that is programmed to the board.

The range code does not apply to the S models, for the are always differential and bipolar.

The *Frequency* and *ClockSource* ADC ActiveX control must be setup before calling the configure function.

EDREADX.Frequency

Frequency	The ADC sampling frequency



WARNING!!

- In normal sampling mode channels are sampled sequentially according to the given channels list. The time spacing between each channel is the same as the frequency in normal mode. The maximum frequency is the same as the maximum speed of the board.
- In burst mode the all channels in the channel list is converted as fast as possible (depends on the A/D converter speed) every period. The period is the same as the sampling frequency. The maximum sampling frequency is the maximum frequency of the board divided by the number of channels in the channel list.

Frequency Example:

Normal Mode	Burst Mode
Frequency = 100 000 Hz Channel List Length = 10 Time = 10 uS Time between channels = 10 uS	Max of Board = 100 000 Hz Frequency = 20 000 Hz Channel List Length = 10 Max Frequency = 2 000 Hz Time = 500 uS Time between channels = 10 uS (ADC Rating) Time between sets = 50 uS

EDREADX.ClockSource

ClockSource	0: Internal and to External Gate 1: Internal 2: External Clock 3: External Clock and Gate

Starting and Stopping the ADC process

A single call is necessary to start or stop the ADC process

API-CALL

Long EDRE_ADStart (uIng Sn)

Parameter	Type	Description
Sn	Unsigned long	Board's serial number
Return	Long	Error Code

ACTIVEX CALL

Long EDREADX.Start ()

Parameter	Type	Description
Return	Long	Error Code

API-CALL
Long EDRE_ADStop (ulng Sn)

Parameter	Type	Description
Sn	Unsigned long	Board's serial number
Return	Long	Error Code

ACTIVEX CALL
Long EDREADX.Stop ()

Parameter	Type	Description
Return	Long	Error Code

Getting data from the driver buffer
A single call is necessary copy data from the driver buffer to the user buffer.

API-CALL
Long EDRE_ADGetData (ulng Sn, plong Buf, pulng BufSize)

Parameter	Type	Description
Sn	Unsigned long	Board's serial number
Buf	Pointer to a long buffer.	Buffer to copy micro voltages too.
BufSize	Pointer to an unsigned long	Size of buffer must be passed or number of samples requested. The returned value will indicate the number of actual samples copied to the buffer.
Return	Long	Error Code

ACTIVEX CALL
Long EDREADX.GetData (plong Buffer, plong Size)

Parameter	Type	Description
Buf	Pointer to a long buffer.	Buffer to copy micro voltages too.
BufSize	Pointer to a long	Size of buffer must be passed or number of samples requested. The returned value will indicate the number of actual samples copied to the buffer.
Return	Long	Error Code

Querying the ADC subsystem
The driver can be queried to check the status of the ADC subsystem. The number of unread samples is one example.

API-CALL

Long EDRE_Query (ulng Sn, ulng QueryCode, ulng Param)

Parameter	Type	Description
Sn	Unsigned long	Board's serial number
QueryCode	Unsigned long	Query code. See appendix Example: ADUNREAD: This will tell you the number of available samples. ADBUSY: Is the ADC subsystem busy?
Param	Unsigned long	Extra parameter.
Return	Long	Returned query code

ACTIVEX CALL

Long EDREADX.GetUnread ()

Parameter	Type	Description
Return	Long	Number of samples available in the driver.

This function automatically queries the ADC driver buffer for the number of available samples.

5

5 Calibration

This chapter contains information to calibrate the A/D and D/A sub-systems of the PCI30FG. The PCI30FG is calibrated during the manufacturing test and therefore does not require recalibration under normal conditions. However under extreme conditions or to optimize accuracy, the board needs to be recalibrated.

Allow the host PC and the board to warm up for at least one hour before calibration.

Requirements

1. Precision voltage source. Range +10V to –10V, with an absolute accuracy better than 0.005%, resolution 100nV or better.
2. Precision digital multimeter with ±10V range, absolute accuracy better than 0.0005%, resolution 100nV or better.
3. Calibration software. This is supplied with the software package.
4. Calibration is only done on channel 1.
5. Use the recommended connector wiring as in figure 7.1.
6. Calibration is performed with the board jumpered into its intended operating mode.
7. Use screened cable and make them as short as possible to reduce noise and loss.

Software

A special software program is required to calibrate the PCI30FG. This software program comes with the PCI30FG and can be found on the EDR Enhanced Software CD. The software is located in the ***utils/pci30fg*** directory.

The program runs under dos and make sure that you do not run it in a Windows command box or on Windows NT. Follow the on screen instructions or the directions in the calibration section.

Connection

Figure 7.1 shows the connection diagram for calibrating your PCI30FG. It is very important that channels that are not used be grounded to analog ground. Also make sure that your voltage source is in perfect working order, because the accuracy of the board will depend on the accuracy of you calibration equipment.

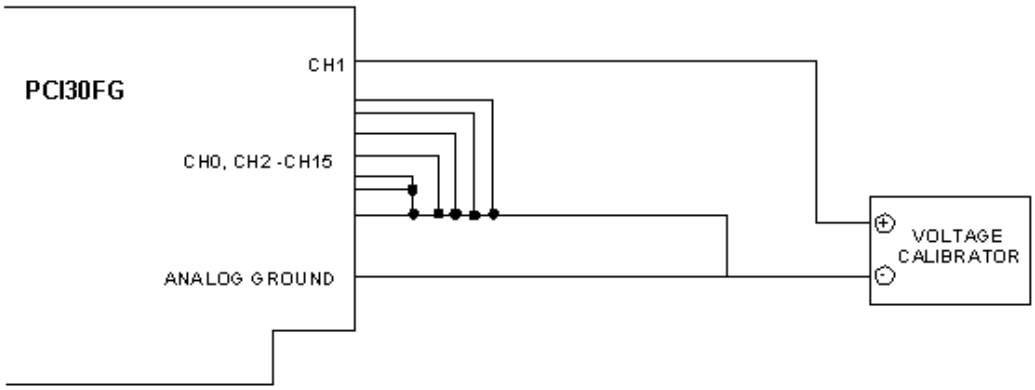


Figure 5-1 A/D Calibration Connections

Variable Resistor Description

Below is a table that shows the function of each pot on the PCI30FG. Only a few are used at a time depending on the version of PCI30FG.

Pot	Description
VR1	A/D OpAmp offset pot – F&G Version
VR2	A/D Bipolar offset pot – G Version
VR3	A/D Monopolar offset pot G Version, Bipolar F(±5V)
VR4	D/A Reference Voltage
VR5	A/D Bipolar gain pot – G Version
VR6	A/D Monopolar gain pot – G Version
VR7	A/D Bipolar gain pot – F Version (±5V)
VR8	A/D Bipolar gain pot – F Version (±10V)
VR9	A/D Bipolar offset pot – F Version (±10V)

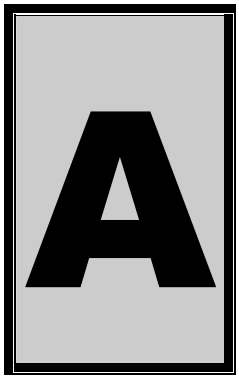
Table 5-1 VR Assignment

A/D Calibrating Procedure

Calibrating the PCI30Gx series

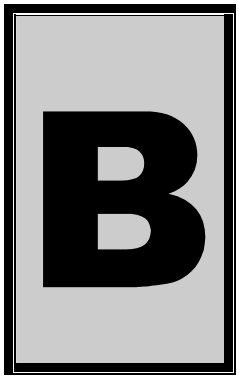
Bipolar Mode

1. Adjust A/D for maximum gain (ie. 1000) and apply 0.00mV to channel 1. All other channels must be connected to analog ground. Adjust VR1, the instrumentation amplifier offset pot, for 800H.
2. Set A/D for a gain of 1 and apply (-FS+2LSB) to channel 1 (ie.-4.9988V for



A. Specification

Specifications where not available on day of print. Please visit our website or request a product datasheet from us.



B. Configuration Constants

Query Codes

Name	Value	Description
APIMAJOR	1	Query EDRE API major version number.
APIMINOR	2	Query EDRE API minor version number.
APIBUILD	3	Query EDRE API build version number.
APIOS	4	Query EDRE API OS type.
APINUMDEV	5	Query number of devices installed.
BRDTYPE	10	Query a board's type.
BRDREV	11	Query a board's revision.
BRDYEAR	12	Query a board's manufactured year.
BRDMONTH	13	Query a board's manufactured month.
BRDDAY	14	Query a board's manufactured day.
BRDSERIALNO	15	Query a board's serial number.
DRVMAJOR	20	Query a driver's major version number.
DRVMINOR	21	Query a driver's minor version number.
DRVBUILD	22	Query a driver's build version number.
ADNUMCHAN	100	Query number of ADC channel.
ADNUMSH	101	Query number of samples-and-hold channels.
ADMAXFREQ	102	Query maximum sampling frequency.
ADBUSY	103	Check if ADC system is busy.
ADFIFOSIZE	104	Get ADC hardware FIFO size.
ADFIFOOVER	105	Check for FIFO overrun condition.
ADBUFFSIZE	106	Check software buffer size.
ADBUFFOVER	107	Check for circular buffer overrun.
ADBUFFALLOC	108	Check if software buffer is allocated.
ADUNREAD	109	Get number of samples available.
ADEXTCLK	110	Get status of external clock line – PCI30FG.
ADEXTTRIG	111	Get status of external trigger line – PCI30FG.
ADBURST	112	Check if burst mode is enabled.
ADRANGE	113	Get ADC range.
DANUMCHAN	200	Query number of DAC channels.
D3AMAXFREQ	201	Query maximum DAC output frequency.
DABUSY	202	Check if DAC system is busy.
DAFIFOSZ	203	Get DAC FIFO size.
CTNUM	300	Query number of counter-timer channels.
CTBUSY	301	Check if counter-timer system is busy.
DIONUMPORT	400	Query number of digital I/O ports.
DIOQRYPORT	401	Query a specific port for capabilities.
DIOPORTWIDTH	402	Get a specific port's width.
INTNUMSRC	500	Query number of interrupts sources.

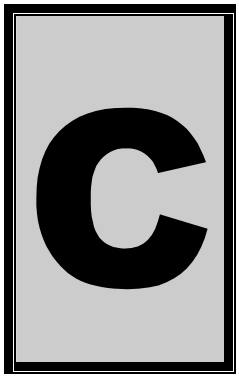
INTSTATUS	501	Queries interrupt system's status.
INTBUSCONNECT	502	Connect interrupt system to bus.
INTISAVAILABLE	503	Check if an interrupt is available.
INTNUMTRIG	504	Check number times interrupted

Error Codes

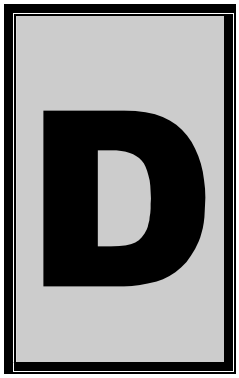
Name	Value	Description
EDRE_OK	0	Function successfully.
EDRE_FAIL	-1	Function call failed.
EDRE_BAD_FN	-2	Invalid function call.
EDRE_BAD_SN	-3	Invalid serial number.
EDRE_BAD_DEVICE	-4	Invalid device.
EDRE_BAD_OS	-5	Function not supported by operating system.
EDRE_EVENT_FAILED	-6	Wait on event failed.
EDRE_EVENT_TIMEOUT	-7	Event timed out.
EDRE_INT_SET	-8	Interrupt in use.
EDRE_DA_BAD_RANGE	-9	DAC value out of range.
EDRE_AD_BAD_CHANLIST	-10	Channel list size out of range.
EDRE_BAD_FREQUECY	-11	Frequency out of range.
EDRE_BAD_BUFFER_SIZE	-12	Data passed by buffer incorrectly sized
EDRE_BAD_PORT	-13	Port value out of range.
EDRE_BAD_PARAMETER	-14	Invalid parameter value specified.
EDRE_BUSY	-15	System busy.
EDRE_IO_FAIL	-16	IO call failed.
EDRE_BAD_ADGAIN	-17	ADC-gain out of range.
EDRE_BAD_QUERY	-18	Query value not supported.
EDRE_BAD_CHAN	-19	Channel number out of range.
EDRE_BAD_VALUE	-20	Configuration value specified out of range.
EDRE_BAD_CT	-21	Counter-timer channel out of range.
EDRE_BAD_CHANLIST	-22	Channel list invalid.
EDRE_BAD_CONFIG	-23	Configuration invalid.
EDRE_BAD_MODE	-24	Mode not valid.
EDRE_HW_ERROR	-25	Hardware error occurred.
EDRE_HW_BUSY	-26	Hardware busy.
EDRE_BAD_BUFFER	-27	Buffer invalid.
EDRE_REG_ERROR	-28	Registry error occurred.
EDRE_OUT_RES	-29	Out of resources.
EDRE_IO_PENDING	-30	Waiting on I/O completion

Digital I/O Codes

Name	Value	Description
DIOOUT	0	Port is an output.
DIOIN	1	Port is an input.
DIOINOROUT	2	Port can be configured as in or out.
DIOINANDOUT	3	Port is an input and an output.



C. Layout Diagram



D. Ordering Information

For ordering information please contact Eagle Technology directly or visit our website www.eagle.co.za. They can also be emailed at eagle@eagle.co.za.

Board	Description
PCI 30-G	16 Channel analog input board @ 100 KHz
PCI 30-GA	16 Channel analog input and 4 channel analog output board @ 100 KHz
PCI 30-G32	32 Channel analog input board @ 100KHz
PCI 30-GA32	32 Channel analog input and 4 channel analog output board @ 100 KHz
PCI 30-F	16 Channel analog input board @ 330 KHz
PCI 30-FA	16 Channel analog input and 4 channel analog output board @ 330 KHz
PCI 30-F32	32 Channel analog input board @ 330 KHz
PCI 30-FA32	132 Channel analog input and 4 channel analog output board @ 330 KHz

Table D-1 Ordering Information

Please visit our website to have a look at our wide variety of data acquisition products and accessories.